

12-Bit High Speed Multiplying D/A Converter

DAC312

FEATURES
Differential Nonlinearity: ±1/2 LSB
Nonlinearity: 0.05%
Fast Settling Time: 250 ns
High Compliance: –5 V to +10 V
Differential Outputs: 0 to 4 mA
Guaranteed Monotonicity: 12 Bits
Low Full-Scale Tempco: 10 ppm/°C
Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS
Low Power Consumption: 225 mW
Industry Standard AM6012 Pinout
Available In Die Form

GENERAL DESCRIPTION

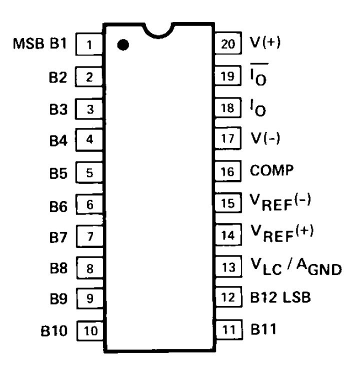
The DAC312 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

The DAC312 combines a 9-bit master D/A converter with a 3-bit (MSBs) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12-bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250 ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

PIN CONNECTIONS

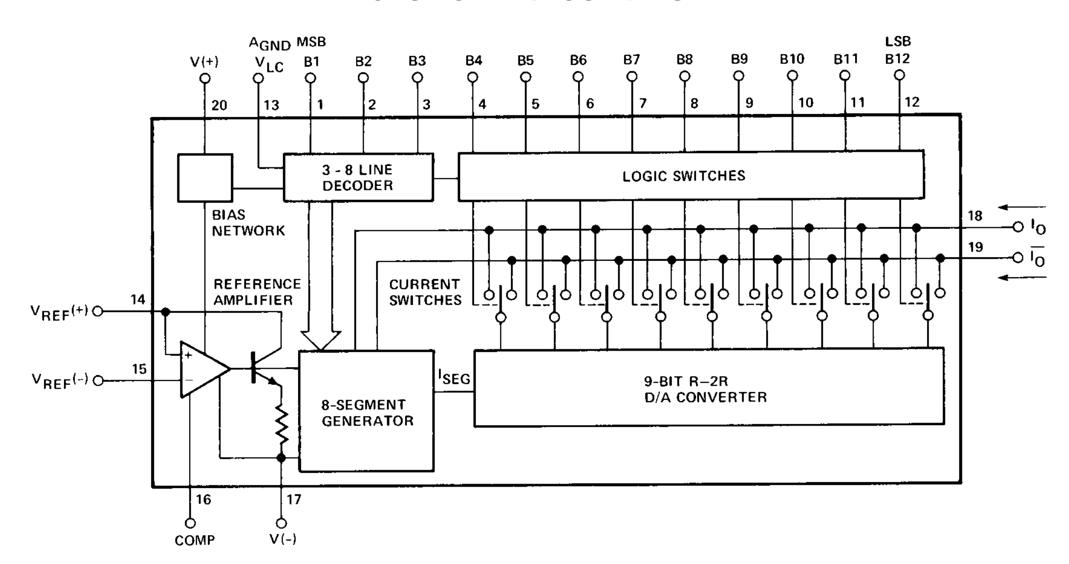
20-Pin Hermetic DIP (R-Suffix), 20-Pin Plastic DIP (P-Suffix), 20-Pin SOL (S-Suffix)



High compliance and low drift characteristics (as low as 10 ppm/°C) are also features of the DAC312 along with an excellent power supply rejection ratio of ±.001% FS/%ΔV. Operating over a power supply range of +5/–11 V to ±18 V the device consumes 225 mW at the lower supply voltages with an absolute maximum dissipation of 375 mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC312 device makes excellent building blocks for A/D converters, data acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

FUNCTIONAL BLOCK DIAGRAM



REV. C

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DAC312–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_S = ±15 V, I_{REF} = 1.0 mA, 0°C ≤ T_A ≤ +70°C for DAC312E and –40°C ≤ T_A ≤ +85°C for DAC312F, DAC312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

			DAC312E			DAC312F			DAC312H			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			12			12			12			Bits
Monotonicity			12			12			12			Bits
Differential Nonlinearity	DNL	Deviation from Ideal			±0.0125			±0.0250			±0.0250	%FS
		Step Size[2]			±0.5			±1			±1	LSB
Nonlinearity	INL	Deviation from Ideal Straight Line[1]			±0.05			±0.05			±0.05	%FS
Full-Scale Current	I_{FS}	V_{REF} = 10 V										
		$R_{14} = R_{15}$ = 10 kΩ[2]	3.967	3.999	4.031	3.935	3.999	4.063	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}			±5	±20		±10	±40		±80		ppm/°C
				±0.005	±0.002		±0.001	±0.004		±0.008		%FS/°C
Output Voltage Compliance	V_{OC}	DNL Specification Guaranteed over Compliance Range	–5		+10	–5		+10	–5		+10	V
Full-Scale Symmetry	I_{FSS}	$\lvert I_{FS}\rvert - \lvert I_{FS}\rvert$		±0.4	±1		±0.4	±2		±0.4	±2	µA
Zero-Scale Current	I_{ZS}				0.10			0.10			0.10	µA
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF[1]		250	500		250	500		250	500	ns
Propagation Delay–All Bits	t_{PLH}	All Bits Switched 50% Point		25	50		25	50		25	50	ns
	t_{PHL}	Logic Swing to 50% Point Output[1]		25	50		25	50		25	50	ns
Output Resistance	R_O			>10			>10			>10		MΩ
Output Capacitance	C_{OUT}			20			20			20		pF
Logic Input												
Levels "0"	V_{IL}	V_{LC} = GND			0.8			0.8			0.8	V
Levels "1"	V_{IH}	V_{LC} = GND	2			2			2			V
Logic Input Current	I_{IN}	V_{IN} = –5 to +18 V			40			40			40	µA
Logic Input Swing	V_{IS}		–5		+18	–5		+18	–5		+18	V
Reference Bias Current	I_{15}		0	–0.5	–2	0	–0.5	–2	0	–0.5	–2	µA
Reference Input Slew Rate	dI/dt	$R_{14(eq)}$ = 800 Ω, C_C = 0 pF[1]	4	8		4	8		4	8		mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = +13.5 V to +16.5 V, V– = –15 V		±0.0005	±0.001		±0.0005	±0.001		±0.0005	±0.001	%FS/%ΔV
	$PSSI_{FS-}$	V– = –13.5 V to –16.5 V, V+ = +15 V		±0.00025	±0.001		±0.00025	±0.001		±0.00025	±0.001	%FS/%ΔV
Power Supply Range	V+	V_{OUT} = 0 V	4.5		18	4.5		18	4.5		18	V
	V–	V_{OUT} = 0 V	–18		–10.8	–18		–10.8	–18		–10.8	V
Power Supply Current	I+	V+ = +5 V, V– = –15 V		3.3	7		3.3	7		3.3	7	mA
	I–	V+ = +15 V, V– = –15 V		–13.9	–18		–13.9	–18		–13 9	–18	mA
	I+	V+ = +5 V, V– = –15 V		3.9	7		3.9	7		3.9	7	mA
	I–	V+ = +15 V, V– = –15 V		–13.9	–18		–13.9	–18		–13.9	–18	mA
Power Dissipation	P_d	V+ = +5 V, V– = –15 V		225	305		225	305		225	305	mW
		V+ = +15 V, V– = –15 V		267	375		267	375		267	375	mW

TYPICAL ELECTRICAL CHARACTERISTICS

@ 25°C; V_S = ±15 V, and I_{REF} = 1.0 mA, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Parameter	Symbol	Conditions	DAC312N Typical	DAC312G Typical	Units
Reference Input Slew Rate	dI/dt		8	8	mA/µs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	25	25	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF.	250	250	ns
Full-Scale	TC_{IFS}		±10	±10	ppm/°C

ELECTRICAL CHARACTERISTICS @ V_S = ±15 V, I_{REF} = 1.0 mA, 0°C ≤ T_A ≤ 70°C for DAC312E and –40°C ≤ T_A ≤ +85°C for DAC312F, DAC312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. *Continued*

			DAC312E			DAC312F			DAC312H			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Logic Input Levels "0"	V_{IL}	V_{LC} = GND			0.8			0.8			0.8	V
Logic Input Levels "1"	V_{IH}	V_{LC} = GND	2			2			2			V
Logic Input Current	I_{IN}	V_{IN} = –5 V to +18 V			40			40			40	µA
Logic Input Swing	V_{IS}		–5		+18	–5		+18	–5		+18	V
Reference Bias Current	I_{15}		0	–0.5	–2	0	–0.5	–2	0	–0.5	–2	µA
Reference Input Slew Rate	dI/dt	$R_{14(eq)}$ = 800 Ω C_C = 0 pF (Note 1)	4	8		4	8		4	8		mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = +13.5 V to +16.5 V, V– = –15 V		±0.0005	±0.001		±0.0005	±0.001		±0.0005	±0.001	%FS/%ΔV
	$PSSI_{FS-}$	V– = –13.5 V to –16.5 V, V+ = +15 V		±0.00025	±0.001		±0.00025	±0.001		±0.00025	±0.001	%FS/%ΔV
Power Supply Range	V+ V–	 V_{OUT} = 0 V	4.5 –18		18 –10.8	4.5 –18		18 –10.8	4.5 –18		18 –10.8	V
Power Supply Current	I+ I– I+ I–	V+ = +5 V, V– = –15 V V+ = +15 V, V– = –15 V		3.3 –13.9 3.9 –13.9	7 –18 7 –18		3.3 –13.9 3.9 –13.9	7 –18 7 –18		3.3 –13.9 3.9 –13.9	7 –18 7 –18	mA
Power Dissipation	P_d	V+ = +5 V, V– = –15 V V+ = +15 V, V– = –15 V		225 267	305 375		225 267	305 375		225 267	305 375	mW

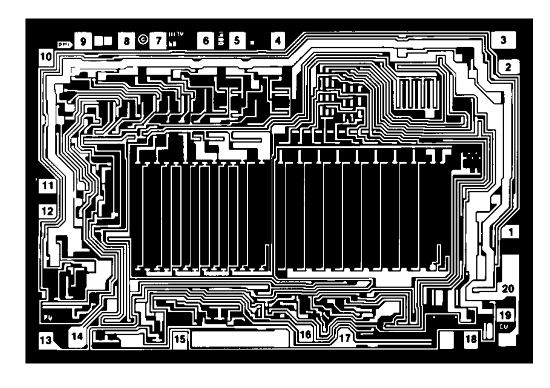
NOTES
[1]Guaranteed by design.
[2]T_A = +25°C for DAC312H grade only.
Specifications subject to change without notice.

WAFER TEST LIMITS @ V_S = ±15 V, I_{REF} = 1.0 mA, T_A = 25°C, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Parameter	Symbol	Conditions	DAC312N Limit	DAC312G Limit	Units
Resolution			12	12	Bits min
Monotonicity			12	12	Bits min
Nonlinearity			±0.05	±0.05	%FS max
Output Voltage Compliance	Voc	Full-Scale Current Change <1/2 LSB	+10 –5	+10 –5	V max V min
Full-Scale Current		V_{REF} = 10.000 V R_{14}, R_{15} = 10.000 kΩ	4.031 3.967	4.063 3.935	mA max mA min
Full-Scale Symmetry	I_{FSS}		±1	±2	µA max
Zero-Scale Current	I_{ZS}		0.1	0.1	µA max
Differential Nonlinearity	DNL	Deviation from Ideal Step Size	±0.012 ±1/2	±0.025 ±1	%FS max Bits (LSB) max
Logic Input Levels “0”	V_{IL}	V_{LC} = GND	0.8	0.8	V max
Logic Input Levels “1”	V_{IH}	V_{LC} = GND	2	2	V min
Logic Input Swing	V_{IS}		+18 –5	+18 –5	V max V min
Reference Bias Current	I_{15}		–2	–2	µA max
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = +13.5 V to +16.5 V, V– = –15 V V– = –13.5 V to –16.5 V, V+ = +15 V	±0.001 ±0.001	±0.001 ±0.001	%/%max
Power Supply Current	I+ I–	V_S = +15 V I_{REF} ≤ 1.0 mA	7 –18	7 –18	mA max
Power Dissipation	P_D	V_S = +15 V I_{REF} ≤ 1.0 mA	375	375	mW max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6
7. B7
8. B8
9. B9
10. B10
11. B11
12. B12 (LSB)
13. V_{LC}/A_{GND}
14. $V_{REF}(+)$
15. $V_{REF}(–)$
16. COMP
17. V–
18. $\overline{I_O}$
19. I_O
20. V+

DIE SIZE 0.141 × 0.096 inch, 13,536 sq. mils (3.58 × 2.44 mm, 8.74 sq. mm)

ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature
- DAC312E . . . . 0°C to +70°C
- DAC312F, DAC312H . . . . –40°C to +85°C

Junction Temperature . . . . –65°C to +150°C
Storage Temperature (Tj) . . . . –65°C to +125°C
Lead Temperature (Soldering, 60 sec) . . . . 300°C
Power Supply Voltage . . . . ±18 V
Logic Inputs . . . . –5 V to +18 V
Analog Current Outputs . . . . –8 V to +12 V
Reference Inputs V_{14}, V_{15} . . . . V– to V+
Reference Input Differential Voltage (V_{14}, V_{15}) . . . . ±18 V
Reference Input Current (I_{14}) . . . . 1.25 mA

Package Type	θ_{JA}[2]	θ_{JC}	Units
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	**27**	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE[1]

Model	DNL	Temperature Range	Package Description	Package Option
DAC312ER[2]	±1/2 LSB	0°C to +70°C	Cerdip-20	Q-20
DAC312FR	±1 LSB	–40°C to +85°C	Cerdip-20	Q-20
DAC312BR/883	±1 LSB	–55°C to +125°C	Cerdip-20	Q-20
DAC312HP	±1 LSB	–40°C to +85°C	Plastic DIP-20	N-20
DAC312HS	±1 LSB	–40°C to +85°C	SOL-20	R-20

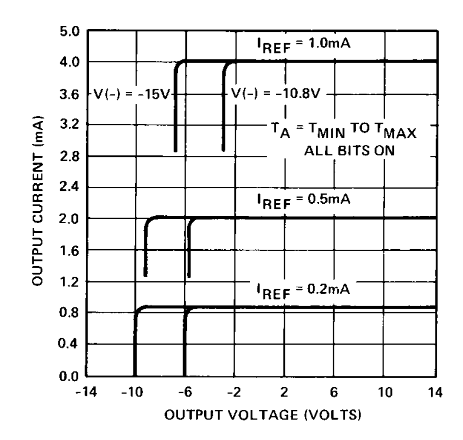
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

CAUTION

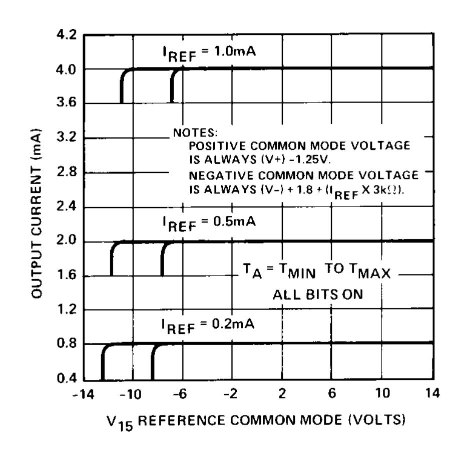
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC312 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



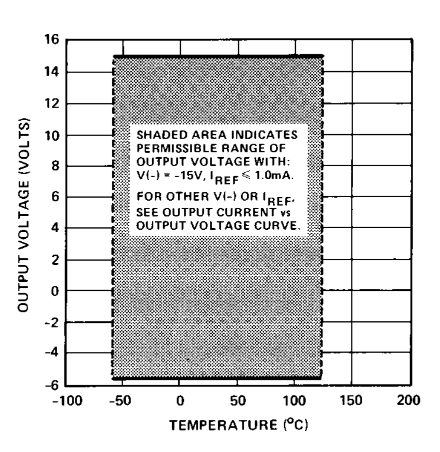
TYPICAL PERFORMANCE CHARACTERISTICS



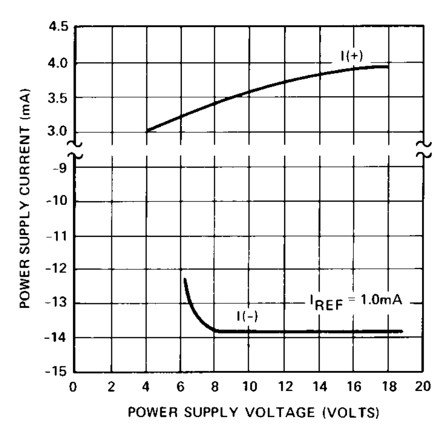
Output Current vs. Output Voltage (Output Voltage Compliance)



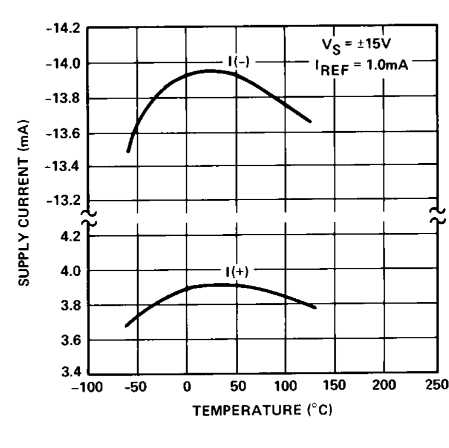
Reference Amplifier Common-Mode Range



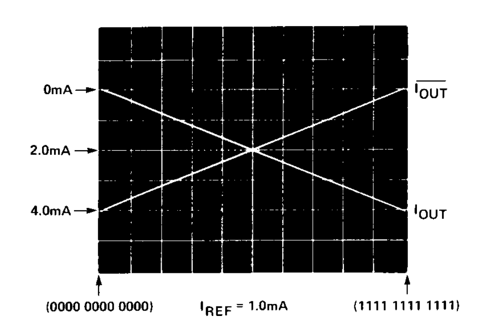
Output Compliance vs. Temperature



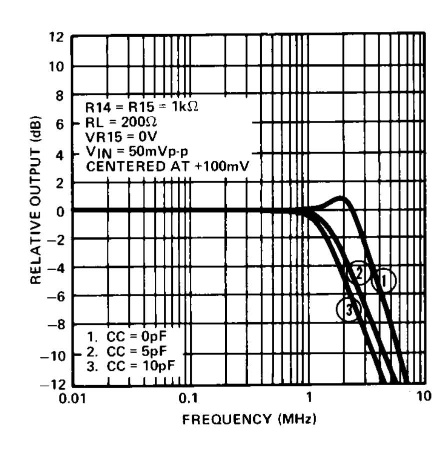
Power Supply Current vs. Power Supply Voltage



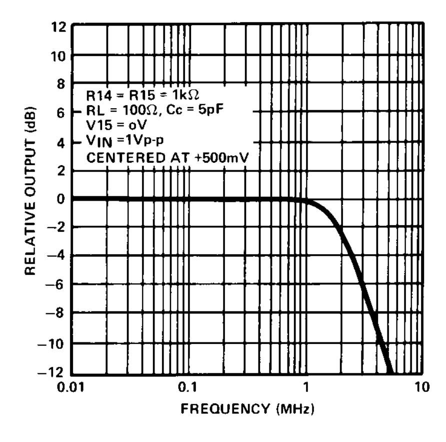
Power Supply Current vs. Temperature



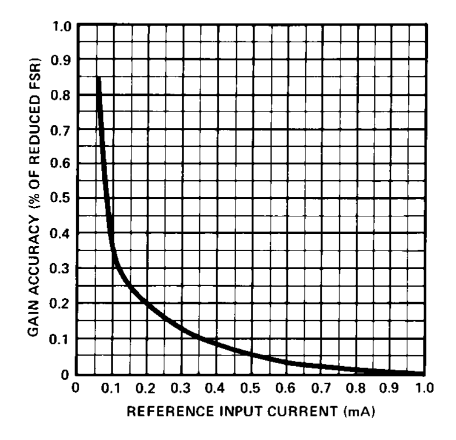
True and Complementary Output Operation



Reference Amplifier Small-Signal Frequency Response

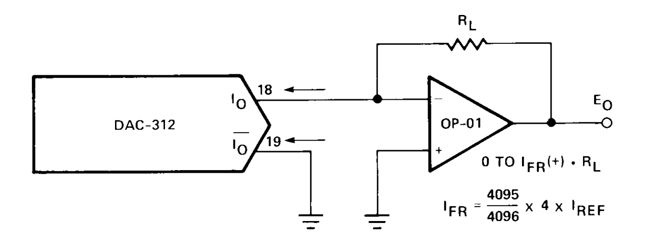


Reference Amplifier Large-Signal Frequency Response

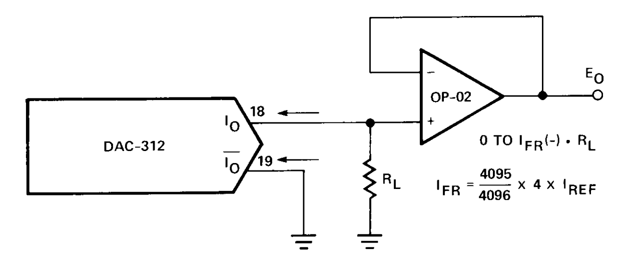


Gain Accuracy vs. Reference Current

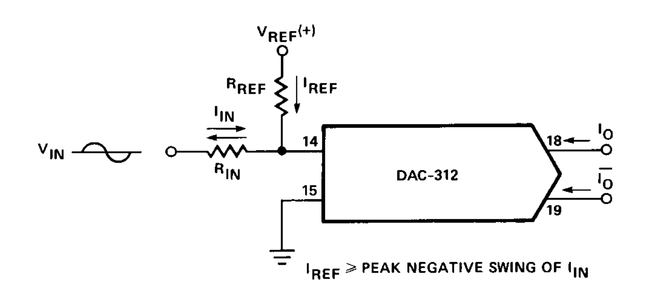
BASIC CONNECTIONS

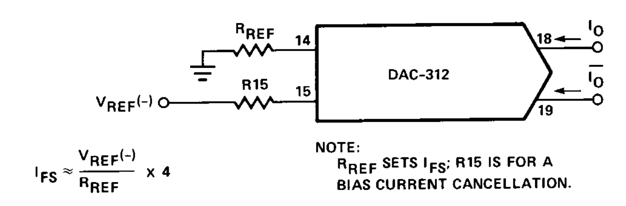


Negative Low Impedance Output Operation

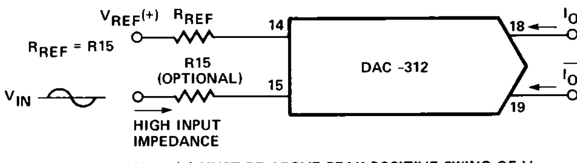


Positive Low Impedance Output Operation

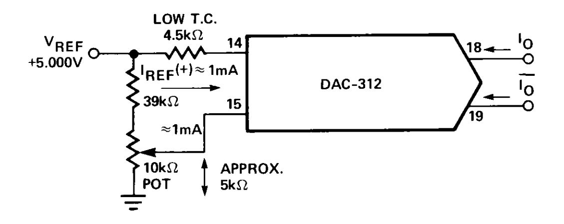




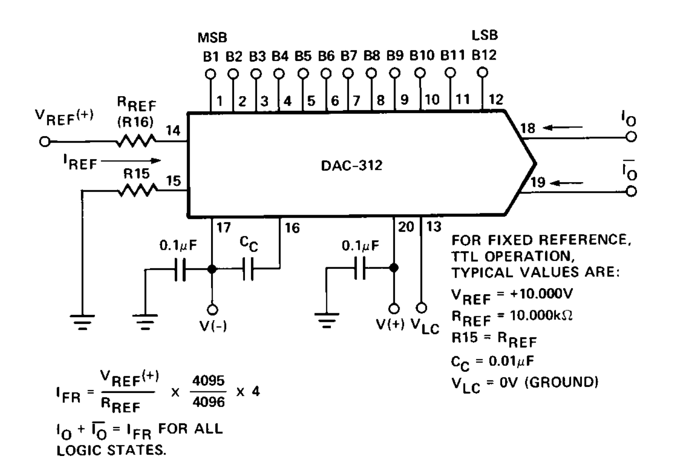
Basic Negative Reference Operation



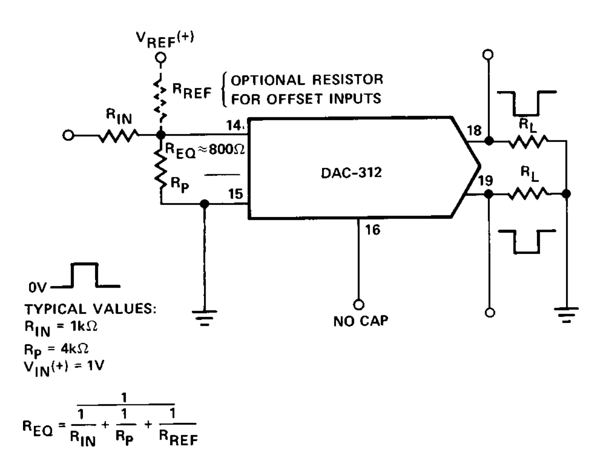
Accommodating Bipolar References



Recommended Full-Scale Adjustment Circuit

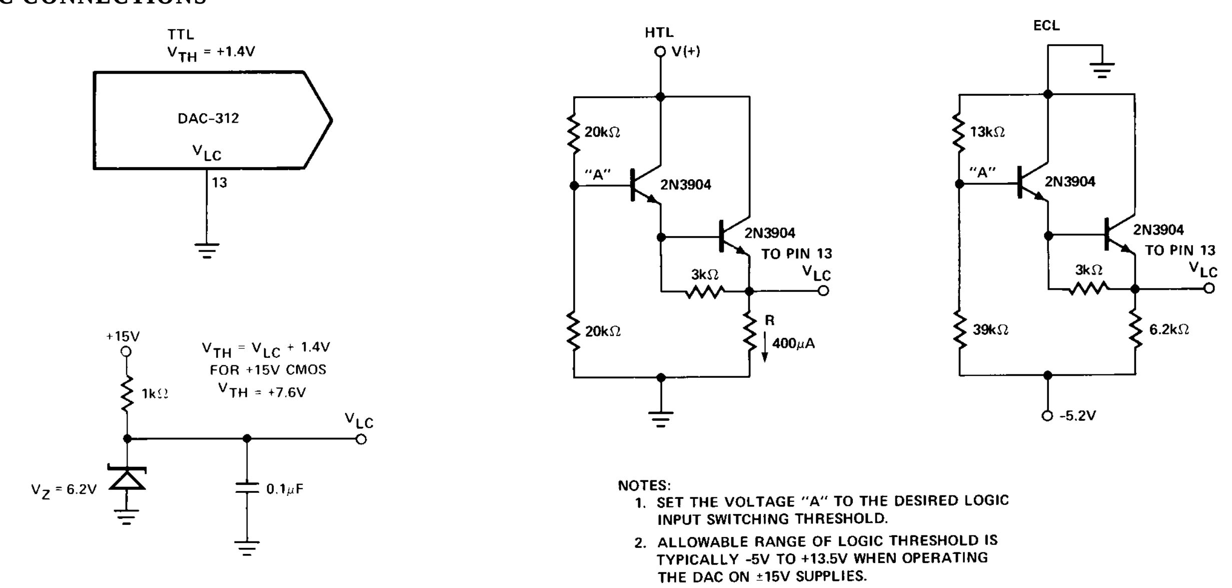


Basic Positive Reference Operation

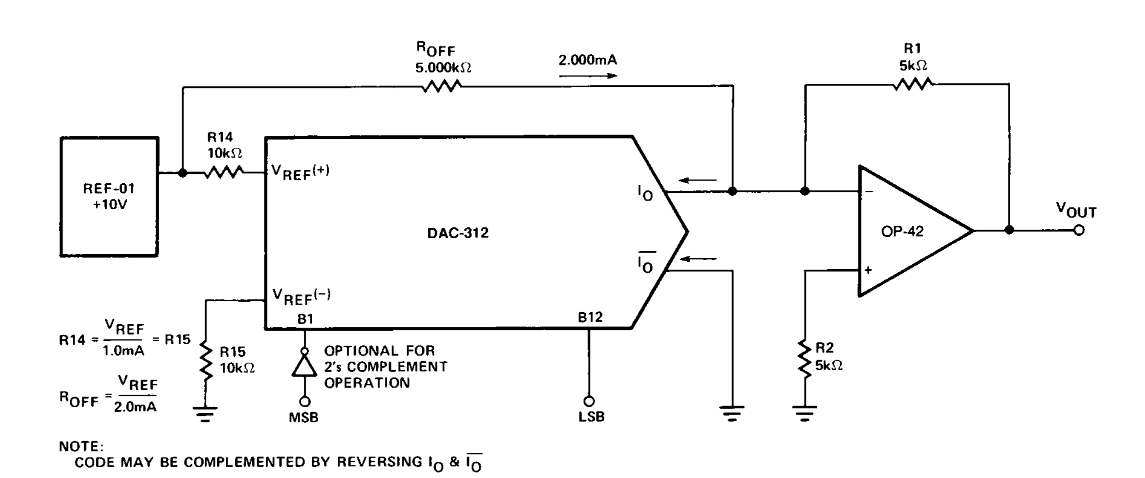


Pulsed Reference Operation

BASIC CONNECTIONS



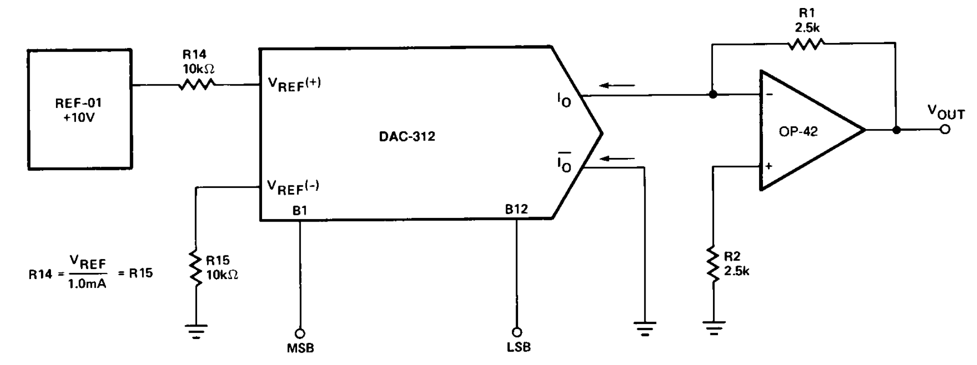
Interfacing with Various Logic Families



Bipolar Offset (True Zero)

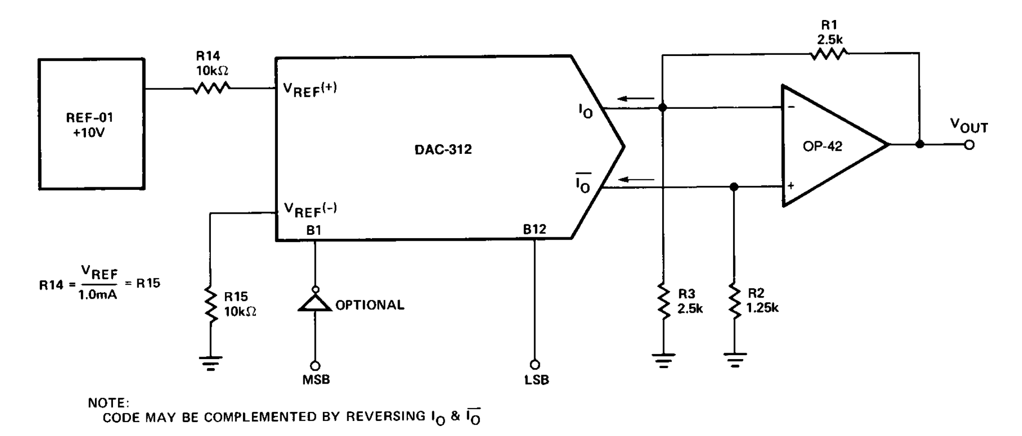
Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Offset Binary; True Zero Output.	Positive Full-Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full-Scale –LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero-Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	–LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
	Negative Full-Scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
	Negative Full-Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000
2s Complement; True Zero Output MSB Complemented (Need Inverter at B1).	Positive Full-Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full-Scale –LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero-Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	–1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
	Negative Full-Scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
	Negative Full-Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000

BASIC CONNECTIONS



Basic Unipolar Operation

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight Binary;	Positive Full-Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
Unipolar with True	Positive Full-Scale –LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
Input Code, True	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	0.0024
Zero Output.	Zero-Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary Binary;	Positive Full-Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
Unipolar with	Positive full-Scale –LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
Complementary Input	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
Code, True Zero Output.	Zero-Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000



Symmetrical Offset Operation

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight Offset Binary;	Positive Full-Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.00	9.9976
Symmetrical about Zero,	Positive Full-Scale –LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
No True Zero Output.	(+) Zero-Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(–) Zero-Scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
	Negative Full-Scale –LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
	Negative Full-Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
1s Complement;	Positive Full-Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
Symmetrical about Zero,	Positive Full-Scale –LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
No True Zero Output.	(+) Zero-Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
MSB Complemented	(–) Zero-Scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
(Need Inverter at B1).	Negative Full-Scale –LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
	Negative Full-Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC312 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0 mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$
$$\text{where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM}-$ = V– plus (I_{REF} × 3 kΩ) plus 1.23 V. The positive common-mode range is V+ less 1.8 V.

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0 V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1 µF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01 µF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC312 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1 mA to 1 µA. Monotonic operation is maintained over a typical range of I_{REF} from 100 µA to 1.0 mA. Although some degradation of gain accuracy will be realized at reduced values of I_{REF}. (See Gain Accuracy vs. Reference Current).

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14 for R14 values of 1.0 Ω, 2.5 Ω and 5.0 kΩ, minimum values of C_C are 5 pF, 10 pF, and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1 kΩ and C_C = 5 pF, the reference amplifier slews at 4 mA/µs enabling a transition from I_{REF} = 0 to I_{REF} = 1 mA in 250 ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 mA to 1 mA) occurs in 62.5 ns when the equivalent impedance at pin 14 is 800 Ω and C_C = 0. This yields a reference slew rate of 8 mA/µs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC312 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40 µA logic input current, and completely adjustable logic threshold voltage. For V– = –15 V, the logic inputs may swing between –5 V and +10 V. This enables direct interface with +15 V CMOS logic, even when the DAC312 is powered from a +5 V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} × 3 kΩ) plus 1.8 V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1 mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 7 mA typical; external circuitry should be designed to accommodate this current.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the true output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25 V above V– and is independent of the positive supply. Negative compliance is +10 V above V–.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC312 operates over a wide range of power supply voltages from a total supply of 20 V to 36 V. When operating with V– supplies of –10 V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9 V with $I_{REF} = 1$ mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8 V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC312 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC312 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10 ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC312 decrease approximately 10% at –55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC312 is capable of extremely fast settling times; typically 250 ns at $I_{REF} = 1.0$ mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25 ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25 ns, with each progressively larger bit taking successively longer. The MSB settles in 250 ns, thus determining the overall settling time of 250 ns. Settling to 10-bit accuracy requires about 90 ns to 130 ns. The output capacitance of the DAC312 including the package is approximately 20 pF; therefore, the output RC time constant dominates settling time if $R_L > 500\ \Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5 mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of the settling time requires the ability to accurately resolve ±1/2 LSB of current, which is ±500 nA for 4 mA FSR. In order to assure the measurement is of the actual settling time and not the RC time of the output network, the resistive termination on the output of the DAC must be 500 Ω or less. This does, however, place certain limitations on the testing apparatus. At I_{REF} values of less than 0.5 mA, it is difficult to prevent RC damping of the output and maintain adequate sensitivity. Because the DAC312 has 8 equal current sources for the 3 most significant bits, the major carry occurs at the code change of 000111111111 to 111000000000. The worst case settling time occurs at the zero to full-scale transition and it requires 9.2 time constants for the DAC output to settle to within ±1/2 LSB (0.0125%) of its final value.

The DAC312 switching transients or "glitches" are on the order of 500 mV-ns. This is most evident when switching through the major carry and may be further reduced by adding small capacitive loads at the output with a minor sacrifice in transition speeds.

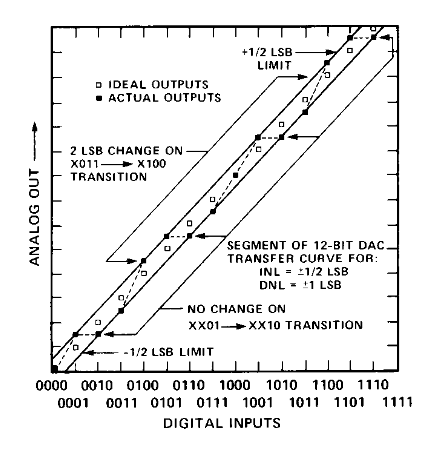
Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 µF capacitors at the supply pins provide full transient protection.

DIFFERENTIAL VS. INTEGRAL NONLINEARITY

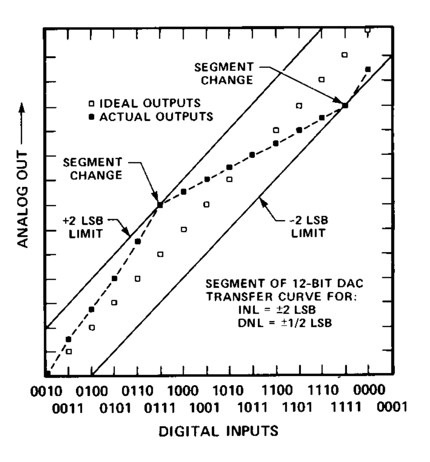
Integral nonlinearity, for the purposes of the discussion, refers to the "straightness"of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The following figures define the manner in which these parameters are specified. The left figure shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT, for example, if the D/A converter output were to be applied to the Y input of a CRT as shown in the application schematic titled "CRT Display Drive." On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with 1/2 LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e., the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2 LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

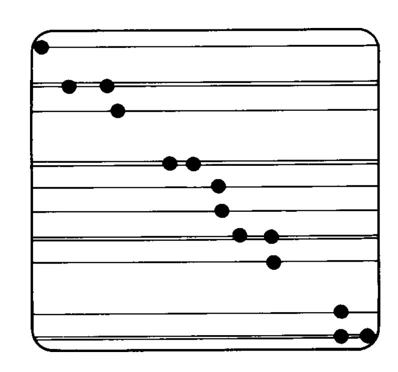
DIFFERENTIAL LINEARITY COMPARISON



D/A Converter with ±1/2 LSB INL, ±1 LSB DNL

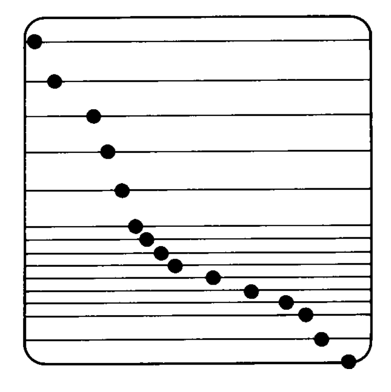


D/A Converter with ±2 LSB INL, ±1/2 LSB DNL



Video Deflection by DACs

ENLARGED "POSITIONAL" OUTPUTS



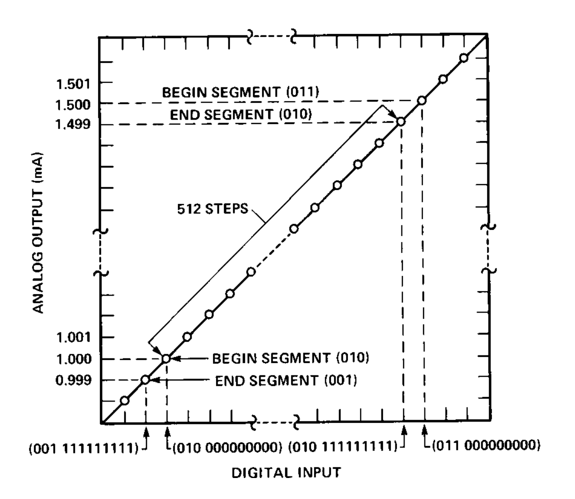
Video Deflection by DACs

ENLARGED "POSITIONAL" OUTPUTS

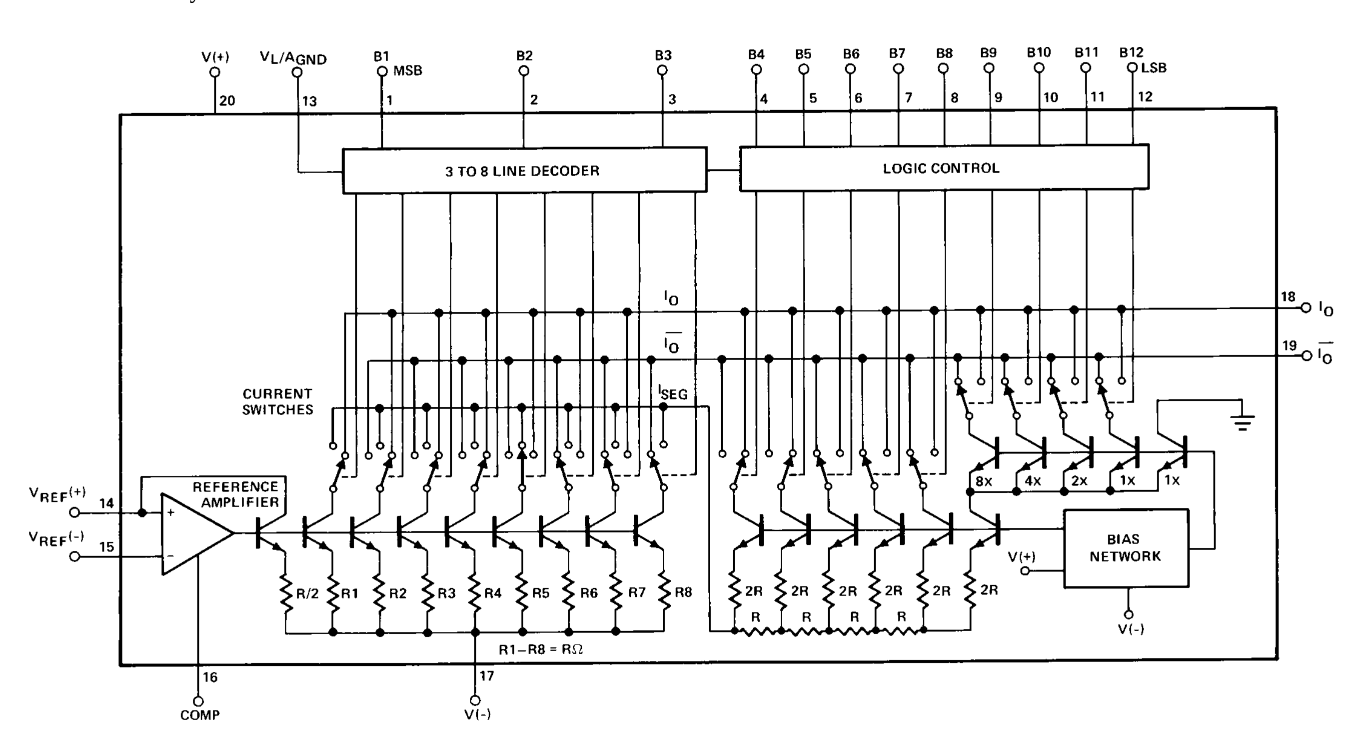
DESCRIPTION OF OPERATION

The DAC312 is divided into two major sections, an 8 segment generator and a 9-bit master/slave D/A converter. In operation the device performs as follows (see Simplified Schematic).

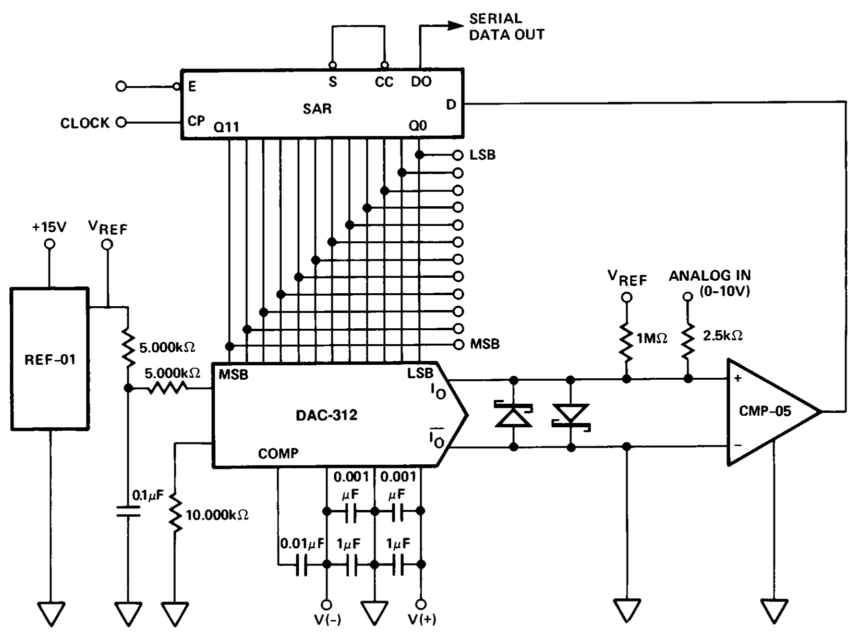
The three most significant bits (MSBs) are inputs to a 3-to-8 line decoder. The selected resistor (R5 in the figure) is connected to the master/slave 9-bit D/A converter. All lower order resistors (R1 through R4) are summed into the I_O line, while all higher order resistors (R6 through R8) are summed into the $\overline{I_O}$ line. The R5 current supplies 512 steps of current (0 mA to 0.499 mA for a 1 mA reference current) which are also summed into the I_O or $\overline{I_O}$ lines depending on the bits selected. In the figure, the code selected is: 100 110000000. Therefore, 2 mA (4 × 0.5 mA/segment) +0.375 mA (from master/slave D/A converter) are summed into I_O giving an I_O of 2.375 mA. $\overline{I_O}$ has a current of 1.625 mA with this code. As the three MSB's are incremented, each successively higher code adds 0.5 mA to $\overline{I_O}$ and subtracts 0.5 mA from I_O, with the selected resistor feeding its current to the master/slave D/A converter; thus each increment of the 3 MSBs allows the current in the 9-bit D/A converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

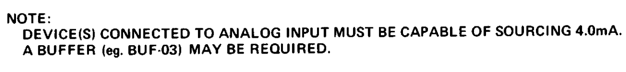


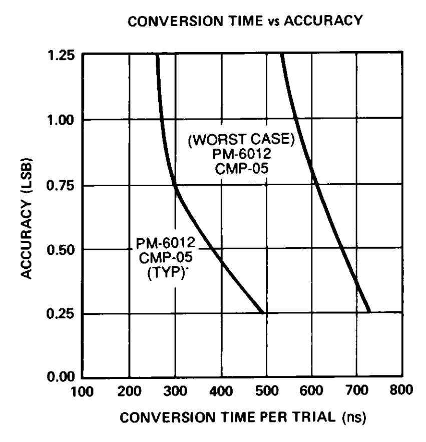
Expanded Transfer Characteristic Segment (001 010 011)



Simplified Schematic




NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA.
A BUFFER (eg. BUF-03) MAY BE REQUIRED.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375nS	680nS
× 13	4.9µS	8.8µS

12-Bit Fast A/D Converter

Outline Dimensions

Dimension shown in inches and (mm).

20-Lead Plastic DIP (N-20)

20-Lead Cerdip (Q-20)

20-Lead Wide Body SOL (R-20)

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